14.8 Fully Integrated CMOS SoC for 56/18/16 CD/DVD-dual/RAM Applications with On-Chip 4-LVDS Channel WSG and 1.5Gb/s SATA PHY

Jyh-Shin Pan, Tse-Hsiang Hsu, Hao-Cheng Chen, Jong-Woei Chen, Bing-Yu Hsieh, Hong-Ching Chen, Wei-Hsuan Tu, Chi-Ming Chang, Roger Lee, Ching-Ho Chu, Yuan-Chin Liu, Chuan-Cheng Hsiao, Chuan Liu, Lily Huang, Chia-Hua Chou, Chang-Long Wu, Meng-Hsueh Lin, Shang-Ping Chen, Brian Liu, Heng-Shou Hsu, Chun-Yiu Lin, Shang-Nien Tsai, Jenn-Ning Yang, Sean Chien, Kuan-Hua Chao, Chang-Po Ma, Yung Cheng, Shu-Hung Chou, Yih-Shin Weng, Ming-Shiam Tsai, Kun-Hung Hsieh, Kuang-Jung Chang, Jin-Chuan Hsu, Hsiu-Chen Peng, Alex Ho

MediaTek, Hsin-Chu, Taiwan

With DVD recording speeds increasing to 16×S or more, the design challenge is to find low cost solutions with high performance and low power consumption. The most promising solution to this challenge is an SoC approach; previous designs, called MFSOC [1] and FESOC [2], have been reported. However, FESOC only supports 8×S DVD operation, and MFSOC does not support 16×S DVD-RAM recording, which has a more complicated structure than other DVD types. Furthermore, both of these previous approaches require a two-chip solution since they do not integrate the RF/AFE processor, and are not optimal from the viewpoints of performance and cost. This paper presents a fully-integrated multi-format SoC (FMSOC), which has recording/decoding capabilities for DVD-ROM/±R/±RW/RAM, DVD±R dual layer, and CD-ROM/R/RW. The SoC accomplishes CD/DVD-dual/RAM operation speed up to 56×S/18×S/16×S, respectively. The maximum channel bit-rate achieves 471Mb/s at 18xS DVD-dual operation.

The block diagram of the FMSOC is illustrated in Fig. 14.8.1. The block RF/AFE synthesizes RF and servo signals according to reflected signals from the optical pickup unit (OPU). A cost effective frequency tuning method for the RF equalizer filter, based on a configurable digital-aided calibration (CDC) architecture with a G_m replica cell (GRC), is proposed. A 1.5Gb/s SATA PHY controller with wide capture range is also integrated. Unlike other solutions, in which the write strategy generator (WSG) is on OPU [3], WSG in the FMSOC is built on-chip with 4 LVDS channels to accomplish 1×S to 18×S DVD recording. A PRML read channel is incorporated for high-speed application. A partial parity (PP) encoding method improves both the efficiency of SDRAM access and the speed of PO parity generation. Advanced power control mechanism (APCM), together with the benefit of RF integration, saves 45% power at 16×S DVD read compared with previous solutions [2].

In the RF equalizer, the CDC makes the cut-off frequency (f_c) of the G_m-C filter insensitive to foundry process and temperature variations. Figure 14.8.2 illustrates the tuning method realized by off-line calibration and on-line G_m tuning. During off-line calibration, a biquad stage of the G_m-C filter is configured as a VCO, whose oscillation frequency (W_{osc}) is proportional to f_c of the filter, and the CDC changes the I-DAC value to adjust W_{osc} of the VCO. That is, f_c of the filter is calibrated to a desired target by altering the G_m value to compensate for capacitor and G_m drift caused by process variation. After off-line calibration, the filter switches to the normal mode, and on-line G_m tuning compensates temperature-induced G_m drift by the internal negative feedback structure of the GRC [4]. CDC significantly reduces the area in contrast to conventional filter tuning methods utilizing PLLs.

A 1.5Gb/s SATA PHY supports wide CDR capture range, which allows RX frequency variance tolerance of +5000/-7500 PPM frequency offset between the reference clock and incoming data due to spread spectrum clocking (SSC). Transmitter PLL enables SSC generation compliant to SATA at -0.5% down spread from the nominal clock over a 31kHz triangular wave period.

Two methods in the FMSOC make issues of high-speed WSG less critical. One is to improve optimal power control. As for the other, the automatic power control (APC) circuit is designed with four separated power-level control circuits to stabilize laser power at high-speed recording. Consequently, real 16×S recording results of 7.5% Data to Clock (DC) jitter reveal the write quality of on-chip WSG in FMSOC is identical to that of on-OPU WSG [3].

In the PRML system, the RF signal through a RF equalizer is sampled with a 6b ADC, which achieves 5.5ENOB at 16×S DVD operation. In addition, a challenge in high-speed DVD-RAM operation is the elaborated L/G and header structure where user data is recorded on both L/G tracks. To switch the polarity of L/G at the correct position, a smart L/G switching mode is incorporated to have more immunity to defective header regions. At 16×S DVD-RAM, the longest settling time of this mode is about 100us.

One of the key attributes of the FMSOC is efficient SDRAM access. As shown in Fig. 14.8.3, an SDRAM is utilized to store ECC data. One DVD ECC block contains 208×182 bytes where each row adopts (182,172) RS codes for inner-code parity (PI) and each column adopts (208,192) RS code for outer-code parity (PO). Suppose that the row page size of the SDRAM is 512B and it takes at least 5 cycles to perform row pre-charge, conventional PO parity generation using Equation (1) does not utilize SDRAM bandwidth well because the ECC data is fetched column by column from the SDRAM, which results in frequent changes of row address. In the FMSOC, the PP encoding method defined by Equation (2) with total 1KB SRAM is used to generate partial PO parity of 32 PO columns at a time. Data of these 32 PO columns are fetched row by row from the SDRAM, in which one 512B SRAM buffer stores source data and the other 512B SRAM buffer stores partial PO parity. To achieve an equivalent SDRAM access efficiency, the necessary SRAM size in PP encoding is 16% of that in the multi-word access (MWA) method [5] and the efficiency of PP encoding is accelerated by 60%.

$$R_j(x) = \sum_{i=192}^{207} B_{i,j}\, x^{207-i} = \left(\sum_{i=0}^{191} B_{i,j}\, x^{191-i}\right) x^{16} \bmod G_{po}(x). \quad (1)$$

$$R^k{}_j(x) = \left(\sum_{i=0}^{15} (R^{k-1}{}_{i,j} + B_{(16*k+i),j})\, x^{15-i}\right) x^{16} \bmod G_{po}(x). \quad (2)$$

where $R^{-1}{}_j(x) = 0, R^{11}{}_j(x) = R_j(x)$ of Equation (1)

APCM is demonstrated in Fig. 14.8.4 where the system clock is from a numerical controlled oscillator (NCO) with a linear step of 1.33MHz. According to the throughput-rate, a minimum frequency detection loop alters the increments of the NCO to control the NCO frequency. As a result, power consumption is minimized while maintaining the required throughput, especially for the case in optical storage systems where data throughput varies with both rotation speed and radius position of OPU. The advantages of NCO are linear step and instantaneous response for frequency updates. When APCM detects the condition that needs a large amount of processing, it temporarily switches NCO to a predetermined fast operation frequency.

The chip is implemented in a 0.18μm 1P6M CMOS process. The 5.4×5.1mm² die has an equivalent transistor count of about 10M. Figure 14.8.5 verifies that the FMSOC achieves 18×S recording for DVD-dual mode. Figure 14.8.6 summarizes chip features, and Fig. 14.8.7 shows the chip micrograph. At 16×S DVD playback, the maximum power consumption is 772mW. Compared with a previous solution [2], which dissipates 1.4W power, a single-chip solution with APCM decreases power consumption by 45% and the operation speed is twice as fast.

References:

[1] J. Pan et al., "A CMOS Multi-Format Read/Write SoC for 7× Blu-ray/16× DVD/56× CD," *ISSCC Dig. Tech. Papers*, pp. 572-573, Feb., 2005.
[2] J. Kim et al., "A 0.18μm CMOS SoC of a front-end hardware platform for DVD-multi recorders," *ICCE Dig. Tech. Papers*, pp. 53-54, Jan., 2005.
[3] Y. Konno et al., "A CMOS 1×- to 16×-Speed DVD Write Channel IC," *ISSCC Dig. Tech. Papers*, pp. 568-569, Feb., 2005.
[4] C. Kim et al., "A CMOS 4x Speed DVD Read Channel IC," *IEEE J. Solid-State Circuits*, pp. 1168-1178, vol. 33, no. 8, Aug. 1998.
[5] C. Tsai et al., "A CMOS SoC for 56/32/56/16 Combo Driver Applications," *ISSCC Dig. Tech. Papers*, pp. 428 -537, Feb., 2004.

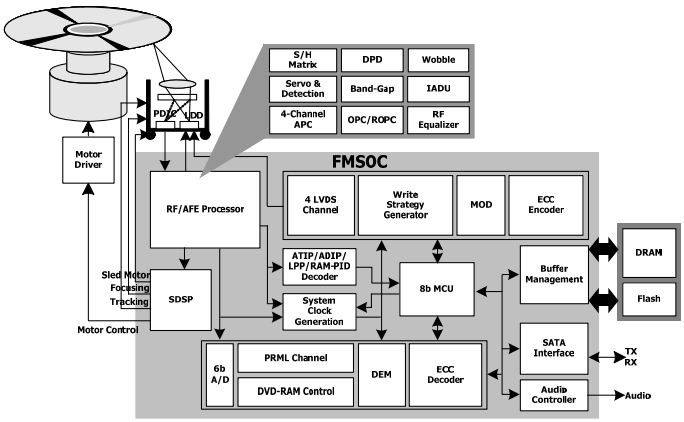

Figure 14.8.1: Block diagram of FMSOC in optical storage system.

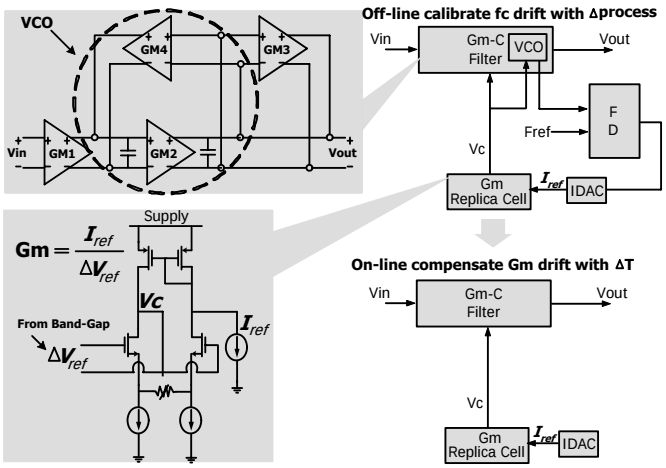

Figure 14.8.2: Configurable digital-aided calibration with a Gm replica cell.

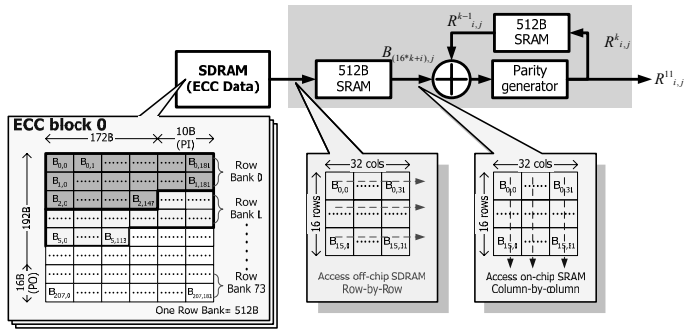

Figure 14.8.3: Illustration of recursive partial PO encode.

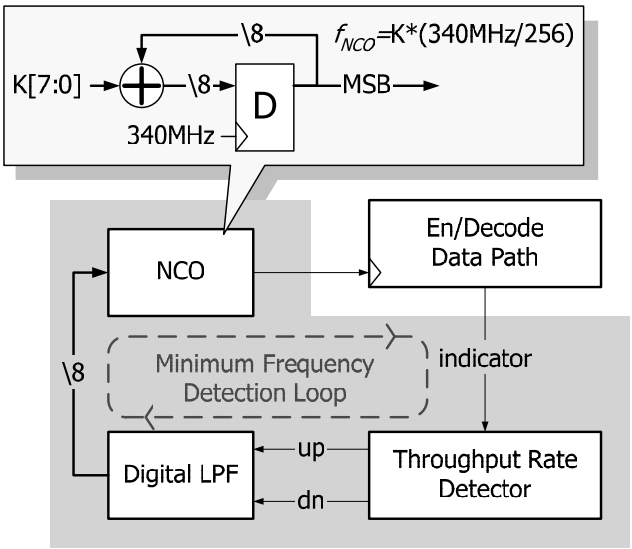

Figure 14.8.4: Advanced power control mechanism.

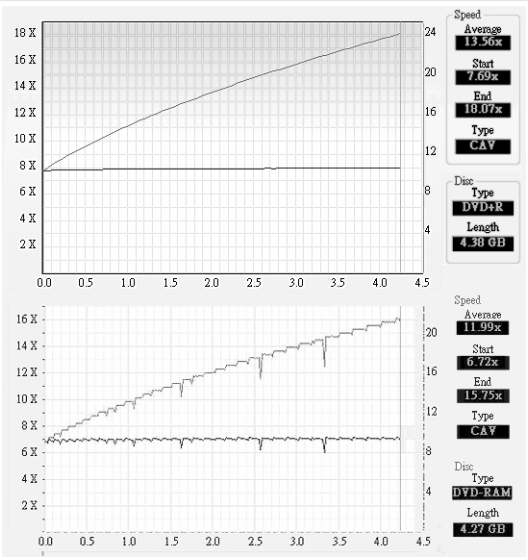

Figure 14.8.5: Transfer rate curves of DVD-dual 18xS write and DVD-RAM 16xS write.

Technology	UMC 0.18μm CMOS 1P6M		
Supply Voltage	1.8V Core, 3.3V Analog & I/O		
Core Area	5.4x5.1mm²		
Transistor Counts	~10M		
Max. working freq.	471MHz		
Package	216 LQFP		
Power Consumption	DVD-R/RW	16xS Write	874mW
	DVD-R/RW/RAM	16xS Read	772mW
	DVD-R with SATA	16xS Read	817mW
	CD 56xS Write		692mW
	CD 56xS Read		664mW

Figure 14.8.6: Chip features.

Continued on Page 653

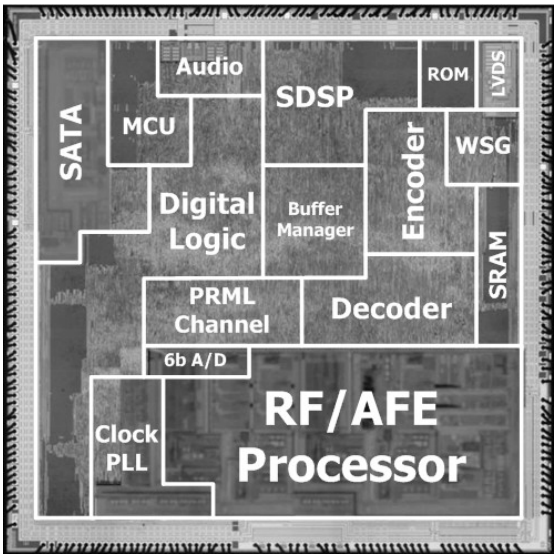

Figure 14.8.7: Die micrograph of FMSOC.

